UNIVERSITY OF THE PUNJAB

B.S. 4 Years Program / Second Semester – 2019

Roll No. in Fig. .....

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Paper: Digital Logic Design

Course Code: IT-104 / IT-12397 Part – I (Compulsory) Time: 15 Min. Marks: 10

ATTEMPT THIS PAPER ON THIS QUESTION SHEET ONLY.

Division of marks is given in front of each question.

This Paper will be collected back after expiry of time limit mentioned above.

Q.1. Encircle the correct option. (10x1=10)

1. According to boolean algebra absorption law, which of following is correct?
   - A. x+xy=x
   - B. (x+y)=xy
   - C. xy+y=x
   - D. x+y=y
2. A binary variable can take values
   - A. 0 only
   - B. 0 and -1
   - C. 0 and 1
   - D. 1 and 2
3. Circuits that employs memory elements in addition to gates is called
   - A. combinational circuit
   - B. sequential circuit
   - C. combinational sequence
   - D. series
4. Full subtract circuits have
   - A. 3 inputs and 2 outputs
   - B. 1 input and 1 output
   - C. both a and b
   - D. None
5. A circuit that converts n inputs to 2^n outputs is called
   - A. encoder
   - B. decoder
   - C. comparator
   - D. carry look ahead
6. Decoder is a
   - A. combinational circuit
   - B. sequential circuit
   - C. complex circuit
   - D. gate
7. One that is not outcome of magnitude comparator is
   - A. a>b
   - B. a-b
   - C. a<b
   - D. a=b
8. 3x8 decoder will have
   - A. 3inputs
   - B. 4inputs
   - C. 5inputs
   - D. 6inputs
9. 4 to 1 mux would have
   - A. 2inputs
   - B. 3inputs
   - C. 4inputs
   - D. 5inputs
10. To design a 4 x 16 Decoder how many 2 x 4 decoder are needed?
    - A. 1
    - B. 2
    - C. 3
    - D. 4

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B.S. 4 Years Program / Second Semester – 2019

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Paper: Digital Logic Design
Course Code: IT-104 / IT-12397 Part – II

Time: 2 Hrs. 45 Min. Marks: 50

ATTEMPT THIS (SUBJECTIVE) ON THE SEPARATE ANSWER SHEET PROVIDED

Question # 2. Short Questions: **(4 x 5 =20 marks)**

a) Convert 2455.30 from Decimal to Octal number system.
b) Perform M-N using r-1's complement where M=1100 and N=1001 are in binary number system.
c) Perform the BCD addition on 259 + 378
d) Draw the truth table for the following.

$$F(A, B, C) = (A'+B')(A'+B'+C')(B+C)$$

e) To implement $F(A,B,C,D) = \Sigma(0,1,2,4,8,9,15)$ using multiplexer with three variables A, B and C as select lines, What size of MUX is required? What size of decoder is required to implement the same function?

Question # 3. Long Questions **(30 marks)**

a) Simplify the following function using K-Map in POS form.

$F=B'D+B'C+ABCD$

$d=A'BD+AB'C'D'$

b) Implement the following function using multiplexer. Keep three variables A, B and D as select lines to the multiplexer.
$F(A,B,C,D) = \Sigma(0,1,2,4,8,9,15)$

c) Draw the logic circuit diagram for 2-bit register using D flip flops capable of performing the following operations:

Control Inputs X_1 X_0	Operation
0 0	Shift Left
0 1	Shift Right
1 0	Complement
1 1	Parallel Load