UNIVERSITY OF THE PUNJAB

B.S. 4 Years Program / Sixth Semester – 2019

Paper: Digital Electronics
Course Code: PHY-310 Part – I (Compulsory) **Time: 15 Min. Marks: 10**

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Signature of Supdt.:

ATTEMPT THIS PAPER ON THIS QUESTION SHEET ONLY.
Division of marks is given in front of each question.
This Paper will be collected back after expiry of time limit mentioned above.

Q.1. Encircle the correct choice. **(1x10=10)**

(i) In the decimal number system, what is the MSD?
(a) the middle digit of a stream of numbers (b) the last digit on the right
(c) the digit to the right of the decimal point (d) the digit with the most weight

(ii) The domain of SOP expression ABC + AB + ABCD + CD is
(a) ABC (b) ABD (c) ACD (d) ABCD

(iii) In a 4-variable K-map, a 2-variable product term is produced by
(a) a 2-cell group of 1s (b) an 8-cell group of 1s
(c) a 4-cell group of 1s (d) a 4-cell group of 0s

(iv) On a K-map, grouping the 0s produces
(a) a product-of-sums expression (b) a sum-of-products expression
(c) a "don't care" condition (d) AND-OR logic

(v) A 5-variable K-map has
(a) sixteen cells (b) thirty-two cells (c) sixty-four cells (d) none as above

(vi) An ADC is an
(a) alphanumeric data coder (b) analog-to-digital comparator
(c) analog device carrier (d) analog-to-digital converter

(vii) How many Flip-Flops are required for mod–16 counter?
(a) 5 (b) 6 (c) 4 (d) 3

(viii) How many clock pulses are required to enter a byte of data serially into an 8-bit shift register?
(a) 8 (b) 4 (c) 16 (d) 9

(ix) An asynchronous counter differs from a synchronous counter in
(a) the number of states in its sequence (b) the method of clocking
(c) the type of flip- flops used (d) the value of the modulus

(x) To serially shift a byte of data into a shift register, there must be
(a) one clock pulse (b) one load pulse
(c) eight clock pulses (d) one clock pulse for each 1 in the data

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Paper: Digital Electronics
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Time: 2 Hrs. 45 Min. Marks: 50

ATTEMPT THIS (SUBJECTIVE) ON THE SEPARATE ANSWER SHEET PROVIDED

Q.2. Write short answers of the following questions: **(2×10 = 20)**

i. Do the following conversions.
   (a) $(650)_{10} = (\ ?\ )_{16}$ (b) $(11000110)_2 = (\ ?\ )_{Gray}$
ii. Subtract the following hexadecimal numbers:
   (a) $94_{16} - 2A_{16}$ (b) $84_{16} - 2A_{16}$
iii. Verify that the NAND operation is commutative.
iv. Sketch K-map for four variables.
v. What is a "Don't Care" condition in a K-map?
vi. By using laws of Boolean algebra, prove that $A + \overline{A}\,B = A + B$
vii. Why D- flip flop is widely used for circuit implementation?
viii. How a J-K flip flop is connected for toggle operation?
ix. Define the term *Shift Registers*.
x. Differentiate between ROM and RAM?

Q.3: (a) Use *K-map* to reduce the following expression to a *minimum SOP* form;

$$\overline{A}\,\overline{B} + A\,\overline{B} + \overline{C}\,\overline{D} + C\,\overline{D}$$

(b) Using Boolean algebra techniques, simplify the expression;

$ABCD + AB\left(\overline{CD}\right) + \left(\overline{AB}\right)CD$, to obtain $CD + AB$.

(5, 5)

Q.4: (a) Describe a method of edge triggering for an *S-R* flip flop.
(b) A device is needed to indicate when one or two HIGH levels occur on its inputs and to produce a LOW output as an indication. Specify the device.

(7, 3)

Q.5: (a) Explain in detail the operation of a 4-bit binary ripple counter.
(b) A 2MHz clock signal is applied to a live stage binary ripple counter. What is the frequency at the fifth flip flop?

(7, 3)